

We claim:

1 1. An active pixel sensor array sampling system comprising:
2 at least one video circuit that generates a video voltage from each one of a
3 group of pixels; and
4 at least one reset circuit that generates a reset voltage associated with each
5 one of the pixels in the group of pixels;
6 wherein one of the at least one video circuit and at least one reset circuit
7 comprises a closed loop sample and hold circuit.

1 2. The system of claim 1 wherein the closed loop sample and hold circuit
2 comprises a single ended common source amplifier.

1 3. The system of claim 1 wherein the closed loop sample and hold circuit
2 comprises a capacitor for holding one of the video voltages and the reset voltages.

1 4. The system of claim 3 wherein the sample and hold circuit includes an
2 amplifier having an input and an output and switches that place its capacitor across
3 its input and output.

1 5. The system of claim 1 wherein the pixels are arranged in columns and
2 rows, the at least one video circuit comprises a plurality of video amplifiers, each
3 video amplifier being associated with a respective column of pixels, and wherein the
4 at least one reset circuit comprises a plurality of reset amplifiers, each reset amplifier
5 being associated with one of the video amplifiers.

1 6. An active pixel sensor array sampling system comprising:
2 a video circuit that generates a video voltage from each one of a group of
3 pixels; and
4 a reset circuit associated with the video circuit that generates a reset voltage
5 associated with each one of the pixels in the group of pixels;
6 wherein the video circuit and the reset circuit each comprise a closed loop
7 sample and hold circuit.

1 7. The system of claim 6 wherein the closed loop sample and hold circuit
2 of each of the video circuit and reset circuit comprises a single ended common
3 source amplifier.

1 8. The system of claim 6 wherein the video and reset closed loop sample
2 and hold circuits each comprise a capacitor for holding the video voltage and the
3 reset voltage respectively.

1 9. The system of claim 6 wherein each of the sample and hold circuits
2 includes an amplifier having an input and an output and switches that place its
3 capacitor across its input and output.

1 10. The system of claim 6 wherein the pixels are arranged in columns and
2 rows and wherein the group of pixels is a column of pixels.

1 11. A video amplifier for use in sampling an active pixel sensor array, the
2 video amplifier comprising a closed loop sample and hold circuit.

1 12. The video amplifier of claim 11 wherein the closed loop sample and
2 hold circuit comprises a single ended common source amplifier.

1 13. The video amplifier of claim 12 wherein the closed loop sample and
2 hold circuit comprises a capacitor for holding a video voltage.

1 14. The video amplifier of claim 13 wherein the sample and hold circuits
2 further includes an amplifier having an input and an output and switches that place
3 the capacitor across the input and output.

1 15. An integrated circuit including a video amplifier for use in sampling an
2 active pixel sensor array, the video amplifier comprising a closed loop sample and
3 hold circuit.

1 16. The integrated circuit of claim 15 wherein the closed loop sample and
2 hold circuit comprises a single ended common source amplifier.

1 17. The integrated circuit of claim 15 wherein the closed loop sample and
2 hold circuit comprises a capacitor for holding a video voltage.

1 18. The integrated circuit of claim 17 wherein the sample and hold circuits
2 further include an amplifier having an input and an output and switches that place the
3 capacitor across the input and output.

1 19. The integrated circuit of claim 15 wherein the integrated circuit is a
2 CMOS integrated circuit.